Remarks

Claims 1-42 were presented for examination. Claim 35 was allowed, claims 1-11, 13-18, 20-25, 27-34 and 36-42 were rejected, and claims 12, 19 and 26 were objected to. Claims 1, 2, 4, 12-17, 19-24, 26-31, 34, 36, 37, 39, 40 and 42 have been amended. Claims 11, 18 and 25 have been cancelled.

Rejections Under 35 U.S.C. § 112

Claims 3 and 8 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 has been amended to provide antecedent basis for the indicated subject matter of claim 3. Applicants believe that claim 3 is no longer indefinite and request that the Examiner withdraw his rejection to claim 3.

Applicants respectfully disagree that claim 8 contains the phrase "said first source/drain region." Therefore, Applicants request that the Examiner withdraw his rejection to claim 8. However, claim 9 does contain the phrase "said first source/drain region." Claim 4 has been amended to provide antecedent basis for the indicated subject matter of claim 9.

Rejections Under 35 U.S.C. § 102(b)

Claims 2-3, 34 and 39 were rejected under 35 U.S.C. § 102(b) as being anticipated by Park. Applicants respectfully traverse.

Claim 2, as amended, recites, in part, a method of making a memory cell by etching a trench in the base substrate, lining the trench with a spacer, depositing a conductive bit line in the trench, etching the bit line back below the uppermost surface of the base substrate and capping

off the trench with a layer of nitride followed by a layer of insulating material.

Park discloses a method of manufacturing a buried bit line DRAM cell by forming the buried bit line in a trench. However, Park fails to disclose capping the bit line with a layer of nitride followed by a layer of insulating material as claimed. Instead, Park discloses capping the bit line with silicon oxide (Col. 5, lines 17-19). Therefore, Applicants believe that claim 2 is not anticipated by Park and request the Examiner withdraw his rejection to claim 2.

Independent claims 34 and 39 as amended, also recite capping the bit line with a layer of nitride followed by a layer of insulating material as called for in claim 2. Therefore, for the same reasons discussed above, Applicants believe claims 34 and 39 are also not anticipated by Park, and request that the Examiner withdraw his rejection of claims 34 and 39.

Claim 3 depends on independent claim 2 and is patentable for the same reasons as independent claim 2 from which it depends. Therefore, Applicants believe claim 3 is also not anticipated by Park, and request that the Examiner withdraw his rejection of claim 3.

Rejections Under 35 U.S.C. § 103(a)

Claims 1, 36 and 40-42 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Park. Applicants respectfully traverse.

Claim 1, as amended, recites a method of making a memory cell by etching a trench in the base substrate, lining the trench with a spacer that is formed by thermally growing a first layer of oxide and depositing a second layer of oxide over said first layer of oxide, depositing a conductive bit line in the trench, and etching the bit line back below the uppermost surface capping off the trench.

Park, as mentioned above, discloses a method of manufacturing a buried bit line DRAM cell by forming the buried bit line in a trench. However, Park fails to disclose forming the spacer by thermally growing a first layer of oxide and depositing a second layer of oxide over said first layer of oxide. Instead, Park discloses depositing a single layer of silicon oxide in the trenches

(Col. 4, lines 64-67; Col. 5, lines 1-4). Because Park does not suggest or teach all the limitations of the claimed invention, Applicants assert that claim 1 is patentable over the prior art and request that the Examiner withdraw his rejection of claim 1.

Independent claims 36, 40 and 42 as amended, also recite forming the spacer by thermally growing a first layer of oxide and depositing a second layer of oxide over said first layer of oxide as recited in claim 1. Therefore, for the same reasons discussed above, Applicants believe claims 36, 40 and 42 are also patentable over Park, and request that the Examiner withdraw his rejection of claims 36, 40 and 42.

Claim 41 depends from independent claim 40 and is patentable for the same reasons as independent claim 40. Therefore, Applicants believe claim 41 is also patentable over Park, and request that the Examiner withdraw his rejection of claim 41.

Claims 4-11, 13-25, 27-33 and 37-38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Park in view Shen. Applicants respectfully traverse.

Claim 4, as amended, recites a method of making a memory cell by etching a trench in the base substrate. The base substrate is comprised of a first base layer and a second base layer. The trench is lined with a spacer. A conductive bit line is deposited in the trench. The bit line is etched back below the uppermost surface of the base substrate and is recessed to at least the uppermost surface of the second base layer of the base substrate. A cap is then formed within the trench over the conductive bit line.

Park, as mentioned above, discloses a method of manufacturing a buried bit line DRAM cell by forming the buried bit line in a trench. However, Park fails to disclose a base substrate comprised of a first base layer and a second base layer.

The Examiner admits Park fails to teach a base substrate with a first base layer and second base layer and cites Shen. However, Shen fails to remedy the deficiencies of Park. Shen discloses an integrated circuit with a buried bit line. Shen also discloses a base substrate comprised of different layers (Col. 4, lines 56-65). However, Shen does not teach or suggest depositing in a trench a conductive bit line and etching back the conductive bit line so that it is recessed to at least the uppermost surface of the second base layer of the base substrate. Therefore, neither Park nor Shen disclose these claimed features of the invention.

Nor does the hypothetical combination of Park and Shen suggest or teach etching back the conductive bit line so that it is recessed to at least the uppermost surface of the second base layer of the base substrate. At best, the hypothetical combination teaches etching back the conductive bit line so that it is below the uppermost surface of the first layer of a multi-layered base substrate. Because the hypothetical combination of Park and Shen does not suggest or teach all the features recited in claim 4, Applicants believe that claim 4 is patentable over the prior art and request the Examiner withdraw his rejection.

Independent claims 10 and 38 also recite etching back the conductive bit line so that it is recessed to at least the uppermost surface of the second base layer of the base substrate. Therefore, for the same reasons discussed above, Applicants believe claims 10 and 38 are also patentable over the hypothetical combination of Park and Shen, and request that the Examiner withdraw his rejection of claims 10 and 38.

Claims 5-9 depend on independent claims 4 and are patentable for the same reasons as independent claim 4 from which they depend. Therefore, Applicants believe claims 5-9 are also patentable over the hypothetical combination of Park and Shen, and request that the Examiner withdraw his rejection of claims 5-9.

Claim 30, as amended, recites a method of making a memory cell forming a p-type well in a base substrate and etching a trench in the base substrate. A transistor is formed in the p-type well. The trench is lined with a spacer. A conductive bit line is deposited within the trench and is etched back so that it is recessed below the uppermost surface of the base substrate by at least a

distance defined by the combined distances of the junction depth plus the depletion width of the transistor.

Park, as mentioned above, discloses a method of manufacturing a buried bit line DRAM cell by forming the buried bit line in a trench. However, Park fails to disclose a first type well within the base substrate. In addition, Park fails to disclose recessing the bit line below the base substrate to a distance of at least the combined distances of the junction depth plus the depletion width of the transistor.

The Examiner admits Park fails to teach a base substrate having an uppermost surface forming a first type well within the base substrate and cites Shen. However, Shen fails to remedy the deficiencies of Park. Shen discloses an integrated circuit with a buried bit line with a first type well within the base substrate. However, Shen fails to disclose recessing the bit line below the base substrate to a distance of at least the combined distances of a junction depth plus the depletion width of the transistor. Therefore, neither Park nor Shen teach or suggest the subject matter claimed in claim 30.

Nor does the hypothetical combination of Park and Shen suggest or teach recessing the bit line below the base substrate to a distance of at least the combined distances of a junction depth plus the depletion width of the transistor. Because the hypothetical combination of Park and Shen does not suggest or teach all the features of the claimed invention, Applicants believe that claim 30 is patentable over the prior art and request the Examiner withdraw his rejection of claim 30.

Independent claims 31, 33 and 37 as amended, also recite recessing the bit line below the base substrate to a distance of at least the combined distances of a junction depth plus the depletion width of the transistor as recited in claim 30. Therefore, for the same reasons discussed above, Applicants believe claims 31, 33 and 37 are also patentable over the hypothetical combination of Park and Shen, and request that the Examiner withdraw his rejection of claims 31, 33 and 37.

Claim 32 depends on independent claim 31 and is patentable for the same reasons as

independent claim 31 from which it depends. Therefore, Applicants believe claim 32 is also patentable over the hypothetical combination of Park and Shen, and request that the Examiner withdraw his rejection of claim 32.

Allowable Subject Matter

Claims 12, 19 and 25 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

Accordingly, claim 12 was amended to incorporate the subject matter of claim 11. Claim 11 was canceled. Claims 13-17 were amended to change their dependency from claim 11 to claim 12.

Claim 19 was amended to incorporate the subject matter of claim 18. Claim 18 was canceled. Claims 20-24 were amended to change their dependency from claim 18 to claim 19.

Claim 26 was amended to incorporate the subject matter of claims 25. Claim 25 was canceled. Claims 27-29 were amended to change their dependency from claim 25 to claim 26. Applicants believe claims 12, 19 and 26 are now in a state of allowance and request that the Examiner withdraw his rejections of claims 12, 19 and 26.

Claims 13-17, 20-24 and 27-29 depend on claims 12, 19 and 26 and are patentable for the same reasons as claims 12, 19 and 26. Therefore, Applicants believe claims 13-17, 20-24 and 27-29 are now in condition for allowance and request that the Examiner withdraw his rejections of claims 13-17, 20-24 and 27-29.

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Conclusion

For the above reasons, Applicants respectfully submit that the above claims represent allowable subject matter. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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